REMARKS

The claims are claims 1 to 9.

Claims 1, 5 and 7 to 9 are further amended. Claims 1 and 5 are amended to explicitly recite the manner of storing the tiles in memory. Claim 7 is amended to recite a second tile cache connected to the second data processor as disclosed in this application at page 5, lines 8 to 19 and illustrated in Figure 2 of this application. Claims 8 and 9 are amended to explicitly recite that the second predetermined number of data words forming each tile is stored in the same DRAM page as taught in the application at page 6, lines 11 to 21.

Claims 1, 2, 4 to 6, 8 and 9 were rejected under 35 U.S.C. 102(e) as being anticipated by Chowdhuri et al.

Claims 1 and 5 recite subject matter not anticipated by Chowdhuri et al. Claim 1 recites "storing image data in tiles in a memory having data words of a predetermined data width, each data word including said first predetermined number of a plurality of pixels adjacently disposed in a single scan line, a set of said second predetermined number of consecutive data words corresponding to a two dimensional tile of the image whereby adjacent data words include pixels of adjacent scan lines, and whereby each tile is stored in said second predetermined number of adjacent data words." Claim 5 similarly recites "a memory storing image data in a plurality of two dimensional tiles, each tile composed of a first predetermined number of pixels adjacently disposed in each scan line of a second predetermined number of adjacent scan lines, said memory having data words of a predetermined data width, each data word including a first predetermined number of a plurality of pixels adjacently disposed on a single scan line, a set of a second predetermined number of consecutive data words corresponding to a two dimensional tile of said first predetermined number of pixels

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and said second predetermined number of scan lines of an image whereby adjacent data words include pixels of adjacent scan lines, and whereby each tile is stored in said second predetermined number of adjacent data words." These recitations differ from the disclosure of Chowdhuri et al.

This language of claims 1 and 5 requires the data to be stored in the memory in tiles. In particular, this language of claims 1 and 5 requires each tile of the image to be stored in a second predetermined number of adjacent data words. Note further, this language requires that all the pixels of one row of a tile be stored in a single data word. These recitations are contrary to the teachings of Chowdhuri et al. Chowdhuri et al states at column 4, line 65 to column 5, line 2:

> "Pseudo tiling provides an impression to the graphics engine that the frame buffer is configured into a tile format, while, in reality, the cache memory, which is seen by the graphics engine, is configured into the tile format and the frame buffer is in scan line format. It should be understood that the term 'pseudo tile' is used when referring to the configuration of the pixel data stored in the frame buffer and the term 'tile' is used when referring to the configuration of the pixel data stored in the cache memory."

Chowdhuri et al states at column 6, lines 21 to 27:

> "It should be understood that the other system components are not affected by the addition of the tile cache 410A as they can still access the frame buffer 125 in standard data format (i.e., scan line format), meaning the other system components are not negatively affected as in the case of tiling the frame buffer itself."

Finally, Chowdhuri et al states at column 7, lines 30 to 32:

> "It should be understood that the frame buffer 125 stays in normal scan line order, but the tile cache 410A is in a tiled configuration."

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Thus these portions of Chowdhuri et al clearly show that data is stored in SDRAM 120A in normal scan order and stored in tile cache 410A in tiles. This storage of data in normal scan order in SDRAM 120A is contrary to the above quoted portions of claims 1 and 5.

Claims 1 and 5 recite further subject matter not anticipated by Chowdhuri et al. Both claims 1 and 5 recite "each data word including said first predetermined number of pixels adjacently disposed in a single scan line." This limitation requires a single data word of the memory to store plural pixels. These plural pixels must be adjacent on a single scan line. Chowdhuri et al includes no teaching regarding the relative length of a data word and a pixel. Chowdhuri et al includes no teaching regarding data words at all. The Examiner's suggestion that the row disclosed in Chowdhuri et al corresponds to the recited data word finds no basis within the reference. Accordingly, claims 1 and 5 are not anticipated by Chowdhuri et al.

The **Response to Arguments** at page 6, line 9 to page 7, line 6 of the OFFICE ACTION includes several assertions obviated by the current amendments to claims 1 and 5. The OFFICE ACTION states at page 6, lines 12 to 14 that claims 1 and 5 do not require the image data to be stored as tiles in the memory. As currently amended claims 1 and 5 explicitly require storage of the image data in the memory as tiles. These claims now also require that "each tile is stored in said second predetermined number of adjacent data words." With these amendments, the arguments presented above correspond to the claim language.

The OFFICE ACTION states at page 6, lines 15 to 19 that claims 1 and 5 do not require "a single data word of the memory to store plural pixels." This portion of the OFFICE ACTION further states that "the predetermined number of pixels could be zero or one." As currently amended claims 1 and 5 explicitly state "each data word

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including a first predetermined number of a plurality of pixels adjacently disposed on a single scan line." This language requires plural pixels per data word and obviates any inference that the number of pixels per data word could be one or zero. With these amendments, the arguments presented above correspond to the claim language.

The OFFICE ACTION states at page 6, line 20 to page 7, line 2 that claims 1 and 5 do not limit "the relative length of a data word as a pixel." As currently amended claims 1 and 5 explicitly state "each data word including a first predetermined number of a plurality of pixels adjacently disposed on a single scan line." This language requires plural pixels per data word and thus explicitly recites the relationship between the data word size and the pixel size. This language obviates any inference that the number of pixels per data word could be one or zero as suggested by the Examiner. With these amendments, the arguments presented above correspond to the claim language.

The OFFICE ACTION states at page 7, lines 3 to 6:

> "With respect to applicant's argument that the examiner's suggestion that the row disclosed in Chowdhuri et al corresponds to the recited data word finds no basis within the reference, examiner respectfully disagrees. Rows of memory inherently contain data words."

The Applicant agrees that the rows of memory in Chowdhuri et al inherently contain data words. However, this is neither the argument made above nor that made in the prior response filed August 18, 2004. The Applicant respectfully submits that Chowdhuri et al includes no teaching regarding the number of pixels stored in a data word. The OFFICE ACTION cites no portion of Chowdhuri et al as allegedly anticipating this limitation. Accordingly, Chowdhuri et al fails to anticipate the recited limitation that "each data word including said first predetermined number of pixels adjacently

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disposed in a single scan line." Accordingly, claims 1 and 5 are not anticipated by Chowdhuri et al.

Claims 8 and 9 recite subject matter not anticipated by Chowdhuri et al. Claim 8 recites the storing step "stores said second predetermined number of adjacent data words in a single page of a dynamic random access memory (DRAM)." Claim 9 recites "said second predetermined number of adjacent data words of each tile are stored in a single page." Both claims 8 and 9 recite that transferring data from memory to tile cache or from tile cache to memory includes "said second predetermined number of page mode DRAM accesses." Chowdhuri et al states at column 6, lines 49 to 61 (including the portion cited in the OFFICE ACTION):

> "SDRAM 120A is selected such that at least one scan line fits into one page of SDRAM.
>
> "As a row of the tile in the tile cache 410A is filled, there is no page miss as the scan line to which the row of pixel data belongs because the pixel data is stored in a single page. When the next row of tile is filled, there is a possibility of a page miss. While accessing the pixel data for the current row, it may be calculated if the next row is going to fall in the same page of the SDRAM 120A. If the next row falls in the same page, then the next row may be accessed without any clock penalty. However, if the next row falls in a separate page, then special action needs to be taken as discussed hereinbelow."

This portion of Chowdhuri et al teaches a different manner of storing the image data in the memory that negates the possibility of transferring tiles in the manner claimed. This portion of Chowdhuri et al includes the qualified statement that page mode accesses are possible "If the next row falls in the same page." Chowdhuri et al further states that "special action needs to be taken" "if the next row falls on a separate page." Because Chowdhuri et al teaches storage in this memory in scan line order, it is virtually certain that a page miss will occur when

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transferring a tile which includes plural scan lines. Thus Chowdhuri et al teaches that page mode accesses may be possible but are not guaranteed. In contrast, claims 8 and 9 recite limitations that guarantee that page mode accesses are possible for every tile. Note further that claims 8 and 9 recite an exact number ("said second predetermined number") of page mode accesses required to transfer a tile. Base claims 1 and 5 recite that this second predetermined number is the number of scan lines in each tile. Chowdhuri et al fails to teach this number of accesses and the OFFICE ACTION fails to point out any portion of Chowdhuri et al as allegedly teaching this number. Accordingly, claims 8 and 9 are allowable over Chowdhuri et al.

Claims 3 and 7 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Chowdhuri et al and Mita et al.

Claims 3 and 7 recite subject matter not made obvious by the combination of Chowdhuri et al and Mita et al. Claim 3 recites "said steps of transferring a tile of image data from the memory into the cache, performing image operations upon said tile of image data transferred to the cache, and transferring said tile of image data from the cache to the memory are performed by different data processors for different tiles." Claim 7 recites a second data processing apparatus and "wherein said data processing apparatus and said second data processing apparatus are programmed to operate upon different tiles of image data simultaneously." Mita et al states at column 24, line 63 to column 25, line 5:

> "The spatial filtering processing will now be described further with reference to the drawings. In the following, a process will be described in which image data in an image memory corresponding to rectangular regions of mXn pixels of an original image are accessed simultaneously, the image data are accepted by an array processor unit (hereinafter referred to as an "APU") comprising mXn processor elements (hereinafter referred to as "PE"), each of which is made to correspond to a

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respective one of the pixels, spatial filtering processing is executed by the APU, and the results are outputted."

Thus each processor element of Mita et al corresponds to a single pixel. Mita et al states at column 33, lines 51 to 64 (cited in the rejection):

"FIG. 57 is a view showing the relationship among an input pixel block 591 corresponding to an original image 590, pixels 591a, a processor unit 592, processor elements 592a, and output image data 593a in an output image memory 593. In accordance with a control signal from a controller 594, the image data block 591 of 16 pertinent pixel elements in the original image memory 590 on the input side are accessed simultaneously, and the image data are accepted by respective ones of the processor elements 592a in the processor unit 562. The processor unit 592 computes typical density information 571 and detail information 572 such as shown in FIG. 55 from the 16 pixels of image data 591, and outputs the results to the image memory 593 on the output side."

This portion of Mita et al makes clear that pixel block 591 consists of pixels 591a. When pixel block 591 is accessed by processor unit 592, individual pixels 591a are processed by processor elements 592a. Thus a single tile (pixel block 591) is processed by a single processor (processor unit 592). Within the single tile are pixels 591a which are processed by processor elements 592a. Mita et al states at column 33, lines 65 to 68 (cited in the rejection):

"The processor elements 592a in the processor unit 592 have one-to-one correspondence with the 4X4 pixels and are arranged in grid fashion in a 4X4 array of 16 elements."

This portion of Mita et al clearly teaches a one-to-one correspondence between pixels 591a and processor elements 592a. Mita et al states at column 34, lines 45 to 60 (cited in the rejection):

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"By repeating the above-described processing through sequentially accessing the original image memory on the input side in 4X4 pixels block units until the compression processing for the final 4X4 pixels block of the original image memory is concluded, compression data equivalent to one page of the original image can be obtained.

"In accordance with the present embodiment as described above, the raw data of the inputted original image, is sequentially accessed every memory block of mXn pixels (e.g. 44 pixels). Therefore, rather than accessing each pixel in the image memory on the input side a plurality of times, mXn pixels of image data can be accessed simultaneously. This makes it possible to transfer the image data while it is being compressed at high speed."

This portion of Mita et al clearly teaches repeated use of a single processing unit 592 to sequentially process pixel blocks 591 of the image 590. Note that processing elements 592a each process a single pixel 591a. This fails to teach the use of plural processors to each process tiles composed of a block of pixels of the image as recited in claims 3 and 7. In order to make obvious the recitations of claims 3 and 7 Mita et al would have to teach or suggest the use of plural processing units 592 operating on different input pixel blocks 591 (Figure 57). Mita et al fails to teach this. Mita el al fails to illustrate or disclose plural processing unit operating on differing pixel blocks. Mita et al always refers to "processing unit" in the singular except for the color plane processing illustrated in Figures 61 and 62. In Figures 61 and 62 of Mita et al the plural processing units are not operating on differing tiles as recited in claims 3 and 7 but are operating on differing color planes of the same tile.

The OFFICE ACTION newly cites Mita et al at Figure 67 and column 38, lines 37 to 53 as making obvious the limitation on plural data processors recited in claims 3 and 7. Regarding Figure 67, Chowdhuri et al states at column 29, lines 52 to 55:

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"FIG. 67 is a view illustrating the correspondence between the elements in the processor elements (PE) group and the pixels in a pixel block of the image memory 317 on the output side."

This disclosure is similar to that noted above in which each processing element operates on a single pixel and not upon a tile of pixels as recited in claims 3 and 7. Chowdhuri et al states at column 38, lines 43 to 48 (included within the portion cited by the Examiner):

"Thereafter, in accordance with the flowchart of FIG. 63, the 4X4 processor elements execute processing in parallel while the processor elements for R, G and B at the same positions, e.g. the processor elements 415, 416, 417, communicate data with one another."

The reference to "at the same positions" negates any inference that this data is different tiles. It is clear that this refers to differing color planes of the same location within the image and thus within the same tile. Accordingly, claims 3 and 7 are not made obvious by the combination of Chowdhuri et al and Mita et al.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. The only amendments made in this response were suggested by the Examiner in the FINAL REJECTION. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early lentry of this amendment, reconsideration and advance to issue are respectfully requested.

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If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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